AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-6 (Cancelled).

7. (Currently Amended) An apparatus for calculating an intermediate value, said apparatus comprising:

a processor connected to a bus;

a graphics controller connected to the bus, said graphics controller including an apparatus including a division stage including a set of result adding devices, connected in series, each having an input and an output, each of said result adding devices to generate an output value that is more precise than its input value, wherein said apparatus is to calculate a final intermediate value is generated that is a value between a first value, X, and a second value, Y, as P*X + (1-P) * Y where P is a non-zero, non-unitary fraction value with an odd number denominator.

8. (Original) The apparatus of claim 7 further comprising a combined multiplication stage coupled to said division stage to generate said intermediate value.

9. (Original) The apparatus of claim 8 wherein said division stage includes a set of add shifting devices, each used for multiplying an input by a base 2 number producing an output.

10. (Original) The apparatus of claim 9 wherein c equals (2^d minus one) divided by said denominator, an integer d is such that said denominator divides (2^d minus one), and an integer m is such that m is a smallest integer where $2^m \geq$ (n plus d) divided by d.

11. (Original) The apparatus of claim 10 wherein said division stage includes:

(1 to m) add shifting devices;

(1 to m) result adding devices where said output of said 1st result adding device is the addition of an output from an adder from said combined multiplication stage and that output shifted (d) places to the left by said 1st add shifting device, and if m is greater than1, then said output of said 2nd result adding device is the addition of said output from said 1st result adding device and that output shifted (2 * d) places to the left by said 2nd add shifting device and continuing in this manner until said output of said (m)th result adding device is the addition of said output of said (m – 1)th result adding device and that output shifted (2^{m-1} * d) places to the left by said (m)th add shifting device; and

a result shifting device used for shifting said output from said (m)th result adding device to the right by (2^{m} * d) places producing said intermediate value.

12. (Currently Amended) An apparatus comprising:

a processor connected to a bus;

a graphics controller connected to the bus, said graphics controller including an apparatus including a combined multiplication stage to multiply a value, X, by a fraction, P, producing a result, where P is a non-zero, non-unitary fraction value with an odd number denominator including a plurality of ANDing devices, each having inputs to receive said value and a setting input to receive a bit signal from a binary representation based on a numerator of said fraction value multiplied by a constant, c, and an adder coupled to outputs of said ANDing devices.

13. (Original) The apparatus of claim 12 further comprising a division stage coupled to said combined multiplication stage to generate said result.

14. (Original) The apparatus of claim 12 wherein said combined multiplication stage includes an incrementing device to produce an output that is an input incremented by one.

15. (Original) The apparatus of claim 14 wherein said combined multiplication stage includes a set of AND shifting devices, each having an input and an output, and each used for multiplying said value by a base 2 number.

16. (Original) The apparatus of claim 15 wherein c equals (2^d minus one) divided by said denominator, an integer d is such that said denominator divides (2^d minus one), and an integer m is such that m is a smallest integer where $2^m \geq$ (n plus d) divided by d.

17. (Original) The apparatus of claim 16 wherein said combined multiplication stage includes:

(1 to d) ANDing devices;

said incrementing device incrementing by one said output of said (d)th ANDing device; and

(1 to d – 1) AND shifting devices where said output of said 1st AND shifting device is said output of said 2nd ANDing device shifted to the left one place and continuing in this manner, said output of said (d – 2)th AND shifting device is said output of said (d – 1)th ANDing device shifted to the left (d - 2) places and finally, said output of said (d – 1)th AND

shifting device is said output of said incrementing device shifted to the left (d – 1) places; and

said adder having (1 to d) inputs to receive said outputs of said (1 to d – 1) AND shifting devices and said output of said 1st ANDing device.

18. (Currently Amended) An apparatus comprising:

a processor connected to a bus;

a graphics controller connected to the bus, said graphics controller including an apparatus including a division stage to multiply a value, X, by a fraction, P, producing a result, where P is a non-zero, non-unitary fraction value with an odd number denominator including a set of result adding devices, connected in series, each having an input and an output, each of said result adding devices generating an output value that is more precise than its input value.

19. (Previously Presented) The apparatus of claim 18 further comprising a combined multiplication stage coupled to said division stage to generate said result.

20. (Original) The apparatus of claim 18 wherein said division stage includes a set of add shifting devices, each used for multiplying an input by a base 2 number producing an output.

21. (Original) The apparatus of claim 20 wherein c equals (2^d minus one) divided by said denominator, an integer d is such that said denominator divides (2^d minus one), and an integer m is such that m is a smallest integer where $2^m \geq$ (n plus d) divided by d.

22. (Original) The apparatus of claim 21 wherein said division stage includes:

(1 to m) add shifting devices;

(1 to m) result adding devices where said output of said 1st result adding device is the addition of an output from an adder from said combined multiplication stage and that output shifted (d) places to the left by said 1st add shifting device, and if m is greater than 1, then said output of said 2nd result adding device is the addition of said output from said 1st result adding device and that output shifted (2 * d) places to the left by said 2^{nd} add shifting device and continuing in this manner until said output of said (m)th result adding device is the addition of said output of said (m – 1)th result adding device and that output shifted (2^{m-1} * d) places to the left by said (m)th add shifting device; and

a result shifting device used for shifting said output from said (m)th result adding device to the right by (2^{m} *d) places producing said intermediate value.

23. (Cancelled).

24. (Cancelled).

25. (Cancelled).

26. (Cancelled).

27. (Cancelled).

28. (Currently Amended) A computer system comprising:

a processor,

a bus connected to said processor,

a graphics controller connected to said bus, said graphics controller ~~comprising~~ :including

----------an apparatus for calculating an intermediate value between a first value, X, and a second value, Y, as P * X + (1 - P) * Y where P is a non-zero, non-unitary fraction value with an odd number denominator, said apparatus ~~comprising~~including:

----------a division stage including a set of result adding devices, connected in series, each having an input and an output, each of said result adding devices generating an output value that is more precise than its input value; and

a display device for displaying output from said graphics controller.

29. (Currently Amended) A computer system comprising:

a processor,

a bus connected to said processor,

a graphics controller connected to said bus, said graphics controller ~~comprising:~~including

----------an apparatus for multiplying a value, X, by a fraction, P, producing a result, where P is a non-zero, non-unitary fraction value with an odd number denominator, said apparatus ~~comprising~~including:

----------a combined multiplication stage including a plurality of ANDing devices, each having inputs to receive said value and a setting input to receive a bit signal from a binary representation based on a numerator of said fraction value multiplied by a constant, c, and an

adder coupled to outputs of said ANDing devices; and

a display device for displaying output from said graphics controller.

30. (Currently Amended) A computer system comprising:

a processor,

a bus connected to said processor,

a graphics controller connected to said bus, said graphics controller ~~comprising:~~including ~~———~~an apparatus for multiplying a value, X, by a fraction, P, producing a result, where P is a non-zero, non-unitary fraction value with an odd number denominator, said apparatus ~~comprising~~including:

~~----------~~a division stage including a plurality of result adding devices, connected in series, each having an input and an output, each of said result adding devices generating an output value that is more precise than its input value; and

a display device for displaying output from said graphics controller.